WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device, comprising:

a memory cell, having a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor source/drain layer region, formed along a first direction within said well, a first gate formed on said semiconductor substrate through a first insulator film, and a second gate formed on said first gate through a second insulator film;

a word line control circuit to drive a word line connected to said second gate;

a program data holding circuit to hold program data;

a programming voltage generator circuit to apply a programming voltage onto a bit line, which is connected to a drain of said semiconductor source/drain layer region; and

a discrimination circuit to verify said program data,

wherein programming of data to said memory cell is conducted by applying positive independent voltages to said second gate and the drain, respectively, while injecting hot electrons generated in a channel portion in a vicinity of the drain when 0V is applied to said well of the first conductivity type and to a source of said semiconductor source/drain layer region, thereby to increase a threshold voltage of said memory cell, and the verification of said programmed data is conducted by applying a verify voltage to said second gate, while applying a positive voltage to the drain and 0V to said well of the first conductivity type and to the source, thereby verifying whether the positive voltage applied to the drain is maintained as it is or

comes down to 0V, depending upon a height of the threshold voltage of said memory cell, by means of said discrimination circuit.

2. The nonvolatile semiconductor memory device, according to claim 1, wherein said discrimination circuit is comprised of a verify circuit of flip-flop type, a first MOS transistor to connect said verify circuit and said bit line in series, and a plurality of MOS transistor groups to convert the data which are verified by said verify circuit, so as to transfer them to said bit line, wherein the verified data are inverted at least one time in a series of operations of said programming and verification.

3. The nonvolatile semiconductor memory device, according to claim 2, wherein said first MOS transistor is comprised of an N-type MOS transistor, a first one of said MOS transistor groups comprised of a second N-type MOS transistor and a third N-type MOS transistor which are connected in series, wherein a gate of said first MOS transistor is connected to a first signal line, a source of said second N-type MOS transistor to said bit line, a source of said third N-type MOS transistor to an internal supply voltage, a gate of said second N-type MOS transistor to a second signal line, and a gate of said third N-type MOS transistor to a first or second output node of said verify circuit of flip-flop type, respectively.

4. The nonvolatile semiconductor memory device, according to claim 2, wherein said first MOS transistor is comprised of an N-type MOS transistor, a first one of said MOS transistor groups is comprised of a second N-type MOS transistor and a P-type MOS transistor which are connected in series, wherein a gate of said

first MOS transistor is connected a first signal line, a source of said second N-type MOS transistor to said bit line, a source of said P-type MOS transistor to an internal supply voltage, a gate of said second N-type MOS transistor to a second signal line, and a gate of said P-type MOS transistor to a first or second output node of said verify circuit of flip-flop type, respectively.

5. The nonvolatile semiconductor memory device, according to claim I, wherein said discrimination circuit is comprised of a verify circuit of flip-flop type, a first MOS transistor to connect said verify circuit and said bit line in series, and a plurality of MOS transistor groups to convert the data which are verified by said verify circuit, so as to transfer said data to said bit line, wherein said first MOS transistor is comprised of an N-type MOS transistor, a first one of said MOS transistor groups is comprised of a second one of said MOS transistor groups comprising a second N-type MOS transistor and a third N-type MOS transistor which are connected in series, and third one of said MOS transistor groups comprising a fourth N-type MOS transistor and a P-type MOS transistor which are connected in series, and wherein a gate of said first MOS transistor is connected to a first signal line, sources of said second N-type MOS transistor and said fourth N-type MOS transistor to said bit line, a source of said third N-type MOS transistor to an internal supply voltage, a source of said P-type MOS transistor to a second internal supply voltage, a gate of said second N-type MOS transistor to a second signal line, a gate of said fourth N-type MOS transistor to a third signal line, and gates of said third N-type MOS transistor and said P-type MOS transistor to an output node of said verify circuit of flip-flop type, respectively.

6. The nonvolatile semiconductor memory device, according to claim 1, wherein said discrimination circuit is comprised of a verify circuit of flip-flop type, a first MOS transistor to connect said verify circuit and said bit line in series, and a plurality of MOS transistor groups to convert the data on the bit line, so as to transfer the data to said verify circuit of flip-flop type, wherein said first MOS transistor is comprised of a N-type MOS transistor, a first one of said MOS transistor groups is comprised of a second N-type MOS transistor and a third N-type MOS transistor which are connected in series, and wherein a gate of said first MOS transistor is connected to a first signal line, a source of said second N-type MOS transistor to an output node of said verify circuit of flip-flop type, a source of said third N-type MOS transistor to an internal supply voltage, and a gate of said second N-type MOS transistor to said bit line, respectively.

7. A nonvolatile semiconductor memory device, according to claim 1, wherein said semiconductor source/drain layer region is a diffusion layer region.